WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

at least one memory cell block of dynamic memory cells arranged in a matrix, the memory cell block including a plurality of word lines;

an address input section for input of a multiple-bit address that includes a row address for selecting one of the plurality of word lines;

a data input/output section for input/output of data corresponding to a memory cell selected by the multiple-bit address; and

a word line activation controller for controlling activation of the word lines;

wherein the word line activation controller comprises:

a row address transition detector for detecting whether the row address has changed;

and wherein the word line activation controller is capable of:

(a) in a first case that the row address transition detector does not detect a change in the row address during consecutive cycles in which at least one of read and write operations of data for the memory cells are enabled and in which an identical row address is used, maintaining an activated state of a word line activated during an initial cycle of the consecutive cycles, without deactivation thereof until a final cycle of the consecutive cycles; and

(b) in a second case that a refresh operation is to be performed during a cycle among the consecutive cycles after the initial cycle, deactivating the activated word line prior to performing the refresh operation.

2. The semiconductor memory device according to claim 1, wherein the address input section is simultaneously supplied with a column address as well as with the row address; and

the row address is assigned to a plurality of uppermost bits of the multiple-bit address.

3. The semiconductor memory device according to claim 1, wherein the semiconductor memory device comprises a plurality of the memory cell blocks; and

the multiple-bit address includes a block address for selecting any one memory cell block from among the plurality of the memory cell blocks;

and wherein the word line activation controller is capable of:

in the first case,

maintaining the activated state of the word line in a first memory cell block activated during the initial cycle, without deactivation thereof until the final cycle;

and additionally, when a read or write operation of data on a memory cell in a second memory cell block different from the first memory cell block is performed during any arbitrary cycle among the consecutive cycles after the initial cycle, maintaining an activated state of a word line in the second memory cell block activated during the arbitrary cycle, without deactivation thereof until the final cycle; and

in the second case,

deactivating the activated word line in the first memory cell block prior to performing the refresh operation in the first memory cell block;

and additionally, when the second memory cell block contains an activated word line, deactivating the activated word line in the second memory cell block prior to performing the refresh operation in the second memory cell block.

4. The semiconductor memory device according to claim 3, wherein, during a cycle in which a read or write operation of data is performed in one memory cell block from among the plurality of memory cell blocks, the refresh operation is performed on memory cell blocks other than the memory cell block on which the read or write operation of data is currently being performed, refreshing of the currently read or written memory cell block being performed during a cycle after the read or write operation has been completed;

and wherein the word line activation controller is capable of, when each of the memory cell blocks being refreshed contains an activated word line, deactivating the activated word line just prior to performing the refresh operation in each of the memory cell blocks.

5. A method for controlling activation of word lines in a semiconductor memory device comprising: at least one memory cell block of dynamic memory cells arranged in a matrix, the memory cell block including a plurality of word lines; an address input section for input of a multiple-bit address that includes a row address for selecting one of the plurality of word

lines; and a data input/output section for input/output of data corresponding to a memory cell selected by the multiple-bit address, wherein:

(a) in a first case that no change in the row address is detected during consecutive cycles in which at least one of read and write operations of data for the memory cells are enabled and in which an identical row address is used, an activated state of a word line activated during an initial cycle of the consecutive cycles is maintained, without deactivation thereof until a final cycle of the consecutive cycles; and

(b) in a second case that a refresh operation is to be performed during a cycle among the consecutive cycles after the initial cycle, the activated word line is deactivated prior to performing the refresh operation.

6. The method according to claim 5, wherein the address input section is simultaneously supplied with a column address as well as with the row address; and

the row address is assigned to a plurality of uppermost bits of the multiple-bit address.

7. The method according to claim 5, wherein the semiconductor memory device comprises a plurality of the memory cell blocks; and

the multiple-bit address includes a block address for selecting any one memory cell block from among the plurality of the memory cell blocks;

and wherein:

in the first case,

the activated state of the word line in a first memory cell block activated during the initial cycle is maintained, without deactivation thereof until the final cycle;

and additionally, when a read or write operation of data on a memory cell in a second memory cell block different from the first memory cell block is performed during any arbitrary cycle among the consecutive cycles after the initial cycle, an activated state of a word line in the second memory cell block activated during the arbitrary cycle is maintained, without deactivation thereof until the final cycle; and

in the second case,

the activated word line in the first memory cell block is deactivated prior to performing the refresh operation in the first memory cell block;

and additionally, when the second memory cell block contains an activated word line, the activated word line in the second memory cell block is deactivated prior to performing the refresh operation in the second memory cell block.

8. The method according to claim 7, wherein, during a cycle in which a read or write operation of data is performed in one memory cell block from among the plurality of memory cell blocks, the refresh operation is performed on memory cell blocks other than the memory cell block on which the read or write operation of data is currently being performed, refreshing of the currently read or written memory cell block being performed during a cycle after the read or write operation has been completed;

and wherein when each of the memory cell blocks being refreshed contains an activated word line, the activated word line is deactivated just prior to performing the refresh operation in each of the memory cell blocks.